

06/25/2003

10/043,237

25jun03 09:24:51 User267149 Session D789.1

SYSTEM:OS - DIALOG OneSearch

File 2:INSPEC 1969-2003/Jun W3

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*File 2: Alert feature enhanced for multiple files, duplicates removal, customized scheduling. See HELP ALERT.

File 6:NTIS 1964-2003/Jun W4

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*File 6: Alert feature enhanced for multiple files, duplicates removal, customized scheduling. See HELP ALERT.

File 8:EI Compendex(R) 1970-2003/Jun W3

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File 34:SciSearch(R) Cited Ref Sci 1990-2003/Jun W4

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File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec

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File 35:Dissertation Abs Online 1861-2003/May

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File 65:Inside Conferences 1993-2003/Jun W4

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File 94:JICST-EPlus 1985-2003/Jun W4

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File 99:Wilson Appl. Sci & Tech Abs 1983-2003/May

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File 144:Pascal 1973-2003/Jun W2

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File 305:Analytical Abstracts 1980-2003/Jun W1

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*File 305: Alert feature enhanced for multiple files, duplicate removal, customized scheduling. See HELP ALERT.

File 315:ChemEng & Biotec Abs 1970-2003/May

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File 350:Derwent WPIX 1963-2003/UD,UM &UP=200340

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File 347:JAPIO Oct 1976-2003/Feb(Updated 030603)

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*File 347: JAPIO data problems with year 2000 records are now fixed. Alerts have been run. See HELP NEWS 347 for details.

File 344:Chinese Patents Abs Aug 1985-2003/Mar

(c) 2003 European Patent Office

File 371:French Patents 1961-2002/BOPI 200209

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*File 371: This file is not currently updating. The last update is 200209.

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Set	Items	Description
S1	30	AU=(DOUMAE, Y? OR DOUMAE Y?)
S2	2	S1 AND IMPLANT????????
S3	2	RD (unique items)
S4	28	S1 NOT S2
S5	0	S4 AND ((FIELD())EFFECT? ?(1W)TRANSIT????????) OR FET? ?)
S6	1	S1 AND (GATE??? (3N) (ELECTRODE? ? OR MICROELECTRODE? ? OR C- ONDUCT????????))
?		

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3/3,AB/1 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus
(c)2003 Japan Science and Tech Corp(JST). All rts. reserv.

03942904 JICST ACCESSION NUMBER: 99A0039740 FILE SEGMENT: JICST-E
Implantation of hydroxyapatite for prevention of collapse in bone
cyst of femoral head in valgus osteotomy.
TAKAHASHI MAKI (1); ENDO NAOTO (1); TOYAMA HIDEKI (1); HORIKOSHI TAIZO (1);
ITO MASAYUKI (1); OGAWA TAISHI (1); **DOUMAE YOICHIRO** (2); SOFUE
MUROTO (3)
(1) Niigata Univ.; (2) Kenritsushibatabyoin; (3) Nakajouchiyuuoubyouin
Hip Jt, 1998, VOL.24, PAGE.464-467, FIG.6, REF.5
JOURNAL NUMBER: X0026AAN ISSN NO: 0389-3634
UNIVERSAL DECIMAL CLASSIFICATION: 616.7-089 615.461/.466
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Short Communication
MEDIA TYPE: Printed Publication

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3/3,AB/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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015269506

WPI Acc No: 2003-330435/200331

XRAM Acc No: C03-085761

XRFX Acc No: N03-264542

MOSFET manufacturing method involves using mask of desired width to defined gate length to **implant** ion in substrate for forming pocket regions

Patent Assignee: OKI ELECTRIC IND CO LTD (OKID); DOUMAE Y (DOUM-I)

Inventor: **DOUMAE Y**

Number of Countries: 002 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030013243	A1	20030116	US 200243237	A	20020114	200331 B
JP 2003031801	A	20030131	JP 2001214613	A	20010716	200331

Priority Applications (No Type Date): JP 2001214613 A 20010716

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
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US 20030013243	A1	12	H01L-021/336		
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JP 2003031801	A	8	H01L-029/78		
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Abstract (Basic): US 20030013243 A1

Abstract (Basic):

NOVELTY - A conductive layer is formed on the main surface of a semiconductor substrate (10). A gate electrode is formed by etching the conductive layer, using a mask which has a desired width to defined gate length. The source and drain regions are formed in the main surface. Multiple pocket regions are formed in the substrate by **implanting** ion in the substrate using the mask.

USE - For manufacturing metal oxide semiconductor field effect transistor MOSFET.

ADVANTAGE - Since the mask of desired width to defined gate length is used, the width of the gate electrode is increased along the downward direction to secure the predetermined gate length after ion **implantation**. The pocket region formed by the ion **implantation** below the gate electrode expand longer by the thickness of the conductive layer.

Therefore the expansion of the depletion layer between the source and drain regions is inhibited efficiently. The FET is formed easily without producing any variation in the electrical characteristics, at a comparatively low impurity concentration.

DESCRIPTION OF DRAWING(S) - The figure shows a cross sectional view illustrating the process of manufacturing FET.

semiconductor substrate (10)
pp; 12 DwgNo 1e/3

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10/043,237

6/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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015269506

WPI Acc No: 2003-330435/200331

XRAM Acc No: C03-085761

XRFX Acc No: N03-264542

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pp; 12 DwgNo 1e/3